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New U.S. Patent Application
Title: ETCHING METHOD
Inventors: 1) Mitsuru ISHIKAWA, 2) Masaaki HAGIHARA, and
3) Koichiro INAZAWA

Sir:

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

1. A check for \$750.00 representing a \$ 710.00 filing fee and \$40.00 for recording the Assignment.
2. Application - 19 pages, including 2 independent claims and 12 claims total.
3. Drawings - 3 sheets of drawings containing 3 figures.
4. Declaration and Power of Attorney.
5. Recordation Form Cover Sheet and Assignment to Tokyo Electron Limited.

Applicants claim the right to priority based on Japanese Patent Application No. 11-303422, filed on October 26, 1999.

Please accord this application a serial number and filing date and record and return the Assignment to the undersigned.

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The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16 or § 1.17 during the pendency of this application to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
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Enclosures

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Title of the Invention

Etching Method

Background of Invention

1 Field of the Invention

The present invention relates to an etching method

2 Description of the Related Art

Reflecting the ever-increasing need for the miniaturization of the wiring structure, organic materials achieving low dielectric constants compared to the dielectric constant of SiO_2 used in the prior art have come to be utilized to constitute a layer insulating film (a film undergoing an etching process) on a Si substrate in the semiconductor manufacturing technology in recent years. Such organic materials with low dielectric constants include, for instance, polyorganosiloxane bridge-formation benzo cyclobutene resin (BCB), SILK (product name) manufactured by Dow Chemicals and FLARE (product name) manufactured by AlliedSignal Incorporated.

Conventionally, CF_4 containing a great quantity of fluorine atoms is used as the etching gas in a dry etching process for forming grooves such as contact holes in an organic material with a low dielectric constant in order to form a reactive seed containing fluorine through plasma discharge or the like, and the processing gas is prepared by mixing in Ar which is mainly used to achieve gas flow rate ratio control and O_2 which is mainly used to achieve an improvement in the penetration, i.e., to promote etching along the depthwise direction.

However, a first problem that should be noted occurring when using the mixed gas containing CF_4 , O_2 and Ar as the processing gas to etch a film constituted of an organic material with a low dielectric constant is a low resist-relative selection ratio. The resist-relative

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selection ratio in this context refers to the value expressed as (average etching rate of the etching target film) / (etching rate of the photoresist) and hereafter it is simply referred to as the "selection ratio." The use of a processing gas with a low selection ratio will result in a wider groove opening and, therefore, is not desirable. It also poses a second problem in that the etching shape is adversely affected by bowing.

Summary of the Invention

An object of that present invention, which has been completed by addressing the problems of the etching method in the prior art discussed above, is to provide a new and improved etching method through which an improvement in the selection ratio and an improvement in the etching shape can be achieved.

In order to achieve the object described above, in a first aspect of the present invention, an etching method for etching an etching target film formed on a substrate placed inside an airtight processing chamber by inducing a processing gas into the processing chamber, in which the processing gas contains at least, CF_4 and N_2 and the etching target film is constituted of an upper organic film containing Si and a lower SiO_2 film as disclosed in claim 1, is provided. It is to be noted that as disclosed in claim 5, the processing gas may further contain Ar.

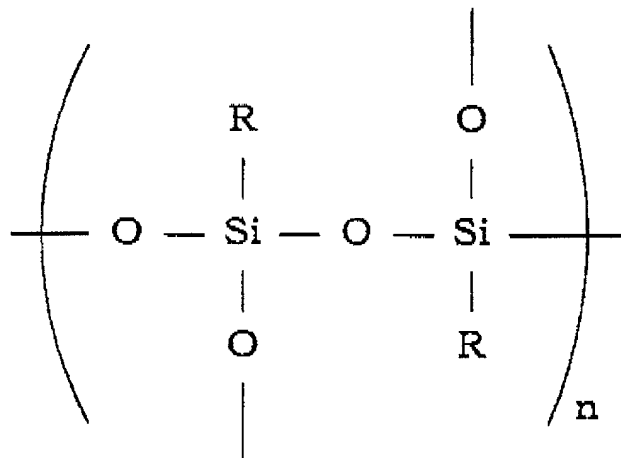
The organic film containing Si (the upper layer film) may be constituted of SiO_2 containing C and H, for instance, as disclosed in claim 2. In addition, the dielectric constant of the organic film containing Si may be set equal to or lower than 3.0, for instance, as disclosed in claim 3. The organic film containing Si may be constituted of organic polysiloxane, for instance, as disclosed in claim 4. Organic polysiloxane as referred to in this context is a substance

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having an SiO₂ bond structure containing a functional group that, in turn, contains C and H, as expressed in the following chemical formula. It is to be noted that in the following chemical formula, the letter R indicates an alkyl group such as a methyl group, an ethyl group or a propyl group or an alkyl group derivative or an allyl group such as a phenyl group or its derivative.

(chemical formula 1)



By adopting this etching method, improvements in the selection ratio and in the etching shape can be achieved. For instance, while the selection ratio achieved by using the mixed gas containing CF₄, O₂ and Ar as a processing gas, as in the prior art, is approximately 2.0, a selection ratio of approximately 5.8 is achieved by using a mixed gas containing CF₄, N₂ and Ar as described above as the processing gas.

In addition, if the flow rate ratio of CF₄ and N₂ (N₂ flow rate / CF₄ flow rate) in the processing gas is less than 1, an etching stop occurs and, as a result, deep etching cannot be achieved. If, on the other hand, (N₂ flow rate / CF₄ flow rate) is larger than 4, bowing tends to occur readily and thus, a good etching shape is not achieved. Accordingly, as disclosed in claim 6, it is desirable to set the flow rate

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ratio of CF_4 and N_2 in the processing gas essentially within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$.

Furthermore, in order to achieve the object described above, in a second aspect of the present invention, an etching method for etching an etching target film formed on a substrate placed inside an airtight processing chamber by inducing a processing gas into the processing chamber, in which the processing gas contains, at least, C_4F_8 and N_2 and the etching target film is constituted of an upper organic film containing Si and a lower SiN film as disclosed in claim 7, is provided.

The organic film containing Si (the upper layer film) may be constituted of SiO_2 containing C and H, for instance, as disclosed in claim 8. In addition, the dielectric constant of the organic film containing Si may be set equal to or lower than 3.0, for instance, as disclosed in claim 9. The organic film containing Si may be constituted of organic polysiloxane, for instance, as disclosed in claim 10.

When the lower layer of the etching target film is constituted of an SiN film, a better selection ratio is achieved by using a mixed gas containing C_4F_8 and N_2 as described above or by using a mixed gas containing C_4F_8 , N_2 and Ar as disclosed in claim 11, rather than by using a mixed gas containing CF_4 and N_2 or a mixed gas containing CF_4 , N_2 and Ar.

In addition, if the flow rate ratio of C_4F_8 and N_2 (N_2 flow rate / C_4F_8 flow rate) in the processing gas is less than 10, an etching stop occurs and, as a result, deep etching is not achieved. Accordingly, it is desirable to set the flow rate ratio of C_4F_8 and N_2 in the processing gas essentially within a range $10 \leq (\text{N}_2 \text{ flow rate} / \text{C}_4\text{F}_8 \text{ flow rate})$ as disclosed in claim 12.

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Brief Description of the Drawings

Further objects and advantages of the invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a sectional view schematically illustrating an etching apparatus which may adopt the present invention;

FIG. 2 schematically illustrates implementation examples 1 of the present invention; and

FIG. 3 schematically illustrates implementation examples 2 of the present invention.

Detailed Description of the Preferred Embodiments

The following is a detailed explanation of preferred embodiments of the etching method according to the present invention, given in reference to the attached drawings. It is to be noted that in the specification and the drawings, the same reference numbers are assigned to components having essentially identical functions and structural features, to preclude the necessity for repeated explanation thereof.

(First Embodiment)

(1) Structure of the etching apparatus

First, in reference to FIG. 1, an etching apparatus 100 in which the etching method in the embodiment is adopted is explained.

A processing chamber 104 is formed inside a processing container 102 which is grounded for safety in the etching apparatus 100 in the figure, and inside the processing chamber 104, a lower electrode 106 constituting a susceptor capable of traveling freely along the vertical direction is provided. An electrostatic chuck 110 connected to a high-voltage DC source 108 is provided at the top of the lower electrode 106, and a workpiece, e.g., a semiconductor wafer

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(hereafter referred to as a "wafer") W is placed on the upper surface of the electrostatic chuck 110. In addition, a focus ring 112 having an insulating property is provided around the wafer W placed on the lower electrode 106. A high-frequency source 120 is connected to the lower electrode 106 via a matcher 118.

At the ceiling of the processing chamber 104 facing opposite the mounting surface of the lower electrode 106, an upper electrode 122 having numerous gas outlet holes 122a is provided. An insulator 123 is provided between the upper electrode 122 and the processing container 102. In addition, a high-frequency source 121 which outputs plasma-generating high-frequency power is connected to the upper electrode 122 via a matcher 119. A gas supply pipe 124 is connected to the gas outlet holes 122a, with first ~ third branch pipes 126, 128 and 130 connected to the gas supply pipe 124 in the example presented in the figure.

A gas supply source 136 which supplies CF_4 is connected to the first branch pipe 126 via a switching valve 132 and a flow-regulating valve 134. A gas supply source 142 that supplies N_2 is connected to the second branch pipe 128 via a switching valve 138 and a flow-regulating valve 140. In addition, a gas supply source 148 that supplies Ar is connected to the third branch pipe 130 via a switching valve 144 and a flow-regulating valve 146. It is to be noted that the inert gas added into the processing gas does not need to be Ar, and any inert gas such as He or Kr may be used as long as the inert gas can be used to adjust the plasma excited inside the processing chamber 104.

Near the bottom of the processing container 102, an evacuating pipe 150 which communicates with a vacuum drawing mechanism (not shown) is connected, and by engaging the vacuum drawing

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mechanism in operation, the atmosphere inside the processing chamber 104 is sustained at a specific reduced pressure.

(2) Structure of the wafer

Next, the structure of the wafer W undergoing the etching process through the etching method in the embodiment is explained.

At the wafer W used in the embodiment, an SiO₂ film (having a dielectric constant of approximately 4.0) to function as an etching stopper for stopping the etching process at a specific depth and also as a protective film that protects the wiring formed on the Si substrate is formed on the Si (silicon) substrate. Above the SiO₂ film, an organic polysiloxane film is formed. In other words, the etching target film in the embodiment is constituted of the organic polysiloxane film constituting the upper layer and the SiO₂ film constituting the lower layer.

It is to be noted that the organic polysiloxane film constituting the upper layer simply represents an example, and the etching target film may be an organic film mainly containing Si, O, R(C and H). For example, the etching target film may be an SiO_2 film containing C and H. More generally, the etching target film may be an organic film containing Si. In addition, while the organic polysiloxane film achieves a dielectric constant of 2.5 ~ 2.7, the etching target film may be, in more general terms, an organic film having a dielectric constant of 3.0 or lower.

An etching mask having a specific pattern is formed on the etching target film. This etching mask may be a mask constituted of, for instance, a photoresist film layer.

Now, the etching process implemented to form contact holes at the wafer W through the etching method in the embodiment by utilizing the etching apparatus 100 described earlier is explained.

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First, the wafer W is placed on the lower electrode 106, the temperature of which has been adjusted to a specific level in advance, and the temperature of the wafer W is sustained within a range of approximately $-20^{\circ}\text{C} \sim 50^{\circ}\text{C}$ in correspondence to the particulars of the processing. For instance, the temperature at the bottoms of the contact holes is sustained at approximately -20°C , the temperature at the openings is sustained at approximately 30°C and the temperature at the sidewalls is sustained at approximately 50°C . In addition, vacuum drawing is implemented inside the processing chamber 104 to ensure that the atmosphere inside the processing chamber 104 achieves a specific pressure suitable for the processing, e.g., approximately 20mTorr (2.67 Pa).

Next, the processing gas in the embodiment, i.e., the processing gas achieved by mixing CF_4 , N_2 and Ar, is induced into the processing chamber 104 by adjusting the flow rates of the individual gases through the flow-regulating valves 134, 140 and 146 inserted at the gas supply pipe 124. During this process, the gas flow rates are adjusted so as to achieve a flow rate ratio within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$ in the processing gas. For instance, the flow rates of N_2 , CF_4 and Ar may be adjusted at approximately 100sccm, 50sccm and 300sccm respectively.

Then, high-frequency power having a frequency of 2 MHz and achieving a power level of approximately 1200 W, for instance, is applied to the lower electrode 106. In addition, high-frequency power having a frequency of approximately 60 MHz and achieving a power level of approximately 1500 W, for instance, is applied to the upper electrode 122. As a result, high-density plasma is generated inside the processing chamber 104, and this plasma forms contact holes achieving a specific shape at the etching target film formed at the wafer W.

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By adopting the embodiment described above, improvements in the selection ratio and the etching shape are achieved. For instance, while a selection ratio of approximately 2.0 is achieved in conjunction with the mixed gas containing CF_4 , O_2 and Ar used as the processing gas in the prior art, a selection ratio of approximately 5.8 is achieved by using the mixed gas containing CF_4 , N_2 and Ar as the processing gas as described above.

In addition, if (N_2 flow rate / CF_4 flow rate) is less than 1, an etching stop occurs and, thus, deep etching cannot be achieved, whereas if (N_2 flow rate / CF_4 flow rate) is larger than 4, bowing tends to occur to result in a poor etching shape. However, since the flow rate ratio of CF_4 and N_2 in the processing gas is set essentially within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$ in the embodiment, an etching stop is prevented and, at the same time, a better etching shape is achieved.

(Second Embodiment)

In the etching method in the first embodiment described above, a mixed gas containing CF_4 , N_2 and Ar is utilized as the processing gas. In this embodiment, a mixed gas containing C_4F_8 , N_2 and Ar is used as the processing gas. The following is a detailed explanation of the second embodiment, given by clarifying the difference from the first embodiment.

While the etching apparatus in which the etching method in the second embodiment is adopted is essentially similar to the etching apparatus 100, a gas supply source 136 that supplies C_4F_8 is connected to the first branch pipe 126 via the switching valve 132 and the flow-regulating valve 134. Thus, the mixed gas containing C_4F_8 , N_2 and Ar is utilized as the processing gas in the embodiment.

Next, the structure of the wafer W to undergo the etching process through the etching method in the embodiment is explained.

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At the wafer W used in the embodiment, an SiN film to function as an etching stopper for stopping the etching process at a specific depth and also as a protective film that protects the wiring formed on an Si substrate is formed on the Si (silicon) substrate. This is a structural feature which differentiates the second embodiment from the first embodiment. In addition, at the top of the SiN film, an organic polysiloxane film is formed. In other words, the etching target film in the embodiment is constituted of the organic polysiloxane film at the upper layer and the SiN film at the lower layer.

In this embodiment, too, the organic polysiloxane film constituting the upper layer simply represents an example, and the etching target film may be an SiO₂ film containing C and H. More generally, the etching target film may be an organic film containing Si. In addition, while the organic polysiloxane film achieves a dielectric constant of 2.5 ~ 2.7, the etching target film may be, in more general terms, an organic film having a dielectric constant of 3.0 or lower.

An etching mask having a specific pattern is formed on the etching target film. This etching mask may be a mask constituted of, for instance, a photoresist film layer, as in the first embodiment.

Now, the etching process implemented to form contact holes at the wafer W through the etching method in the embodiment is explained.

First, the wafer W is placed on the lower electrode 106, the temperature of which has been adjusted to a specific level in advance, and the temperature of the wafer W is sustained within a range of approximately -20°C ~ 50°C in correspondence to the particulars of the processing. For instance, the temperature at the bottoms of the contact holes is sustained at approximately -20°C, the temperature at the openings is sustained at approximately 30°C and the temperature at the sidewalls is sustained at approximately 50°C. In addition,

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vacuum drawing is implemented inside the processing chamber 104 to ensure that the atmosphere inside the processing chamber 104 achieves a specific pressure suitable for the processing, e.g., approximately 20mTorr (2.67 Pa), as in the first embodiment.

Next, the processing gas in the embodiment, i.e., the processing gas achieved by mixing C_4F_8 , N_2 and Ar, is induced into the processing chamber 104 by adjusting the flow rates of the individual gases through the flow-regulating valves 134, 140 and 146 inserted at the gas supply pipe 124. During this process, the gas flow rates are adjusted so as to achieve a flow rate ratio within a range of $10 \leq (N_2 \text{ flow rate} / C_4F_8 \text{ flow rate})$ in the processing gas. For instance, the flow rates of N_2 , C_4F_8 and Ar may be adjusted at approximately 200sccm, 12sccm and 300sccm respectively.

Then, high-frequency power having a frequency of 13.56 MHz and achieving a power level of approximately 1200 W, for instance, is applied to the lower electrode 106. In addition, high-frequency power having a frequency of approximately 60 MHz and achieving a power level of approximately 1500 W, for instance, is applied to the upper electrode 122. As a result, high-density plasma is generated inside the processing chamber 104, and this plasma forms contact holes achieving a specific shape at the etching target film formed at the wafer W, as in the first embodiment.

When the lower layer of the etching target film is constituted of an SiN film as in this embodiment, a better selection ratio is achieved by using the mixed gas containing C_4F_8 , N_2 and Ar rather than by using a mixed gas containing CF_4 , N_2 and Ar.

In addition, while if $(N_2 \text{ flow rate} / C_4F_8 \text{ flow rate})$ is less than 10, an etching stop occurs and, therefore, deep etching cannot be achieved, the flow rate ratio of C_4F_8 and N_2 in the processing gas is

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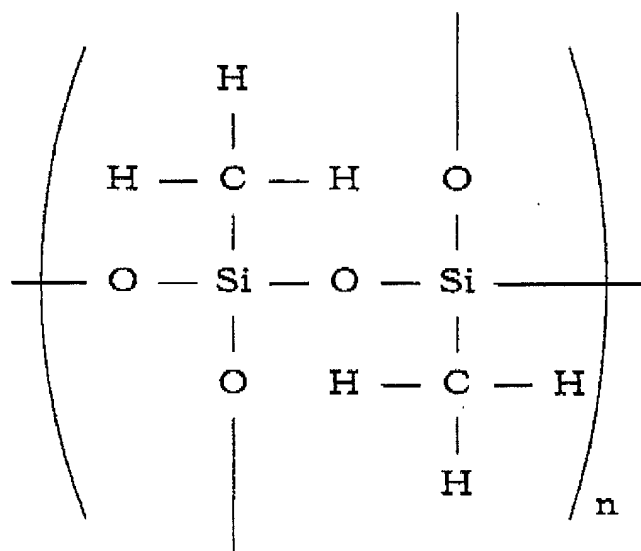
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essentially set within a range of $10 \leq (\text{N}_2 \text{ flow rate} / \text{C}_4\text{F}_8 \text{ flow rate})$ in the embodiment, to prevent such an etching stop from occurring.

(Implementation Examples)

Next, examples of implementation of the etching method according to the present invention are explained in reference to FIG. 2 and FIG. 3. It is to be noted that in the implementation examples, contact holes are formed at the etching target film at the wafer W by employing the etching apparatus 100 explained in reference to the embodiments, and therefore, the same reference numbers are assigned to components having roughly identical functions and structural features to those in the etching apparatus 100 and the wafer W explained earlier, to preclude the necessity for repeated explanation thereof. In addition, the etching process conditions are set roughly the same as those in the embodiments. It is to be noted that organic polysiloxane constituting the upper layer of the etching target film achieves the following structure.

(chemical formula 2)



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(A) Implementation examples 1 (changes in the flow rate ratio of CF_4 and N_2)

In these implementation examples, the processing gas is constituted of a mixed gas containing CF_4 , N_2 and Ar and the flow rate ratio of CF_4 and N_2 is varied.

In implementation examples 1(a) ~ 1(c), an etching process is implemented by adjusting the flow rate ratio of CF_4 , N_2 and Ar, respectively at (a) 50:200:300, (b) 50:100:300 and (c) 50:50:300, to form contact holes at the layer insulating film of the wafer W. The results achieved in the individual implementation examples are presented in FIG. 2. FIG. 2(A) shows the state at the central area of the wafer W achieved in implementation example 1(a), FIG. 2 (B) shows the state at the edge of the wafer W achieved in implementation example 1(a), FIG. 2(C) shows the state at the central area of the wafer W achieved in implementation example 1(b), FIG. 2(D) shows the state at the edge of the wafer W achieved in implementation example 1(b), FIG. 2(E) shows the state at the central area of the wafer W achieved in implementation example 1(c) and FIG. 2 (F) shows the state at the edge of the wafer W achieved in implementation example 1(c).

As shown in FIG. 2, a bowing X occurs at (a) CF_4 : N_2 = 50:200, and therefore, the etching shape is poor. A high selection ratio and a good etching shape are achieved at (b) CF_4 : N_2 = 50:100. At (c) CF_4 : N_2 = 50:50, the selection ratio is lower than that achieved at (b) and also, an etching stop occurs.

Thus, among these implementation examples, the flow rate ratio (b) CF_4 : N_2 = 50:100 = 1:2 achieves the most desirable results, and by comparing the results at (a) ~ (c), it can be judged that a higher resist-relative selection ratio and a good etching shape are achieved when the flow rate ratio is set essentially within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$.

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(B) Implementation examples 2 (changes in the flow rate ratio of C_4F_8 and N_2)

In this implementation example, the processing gas is constituted of a mixed gas containing C_4F_8 , N_2 and Ar and the flow rate ratio of C_4F_8 and N_2 is varied.

In implementation examples 2(a) ~ 2(b), an etching process is implemented by adjusting the flow rate ratio of C_4F_8 , N_2 and Ar, respectively at (a) 12:200:300 and (b) 12:100:300 to form contact holes at the layer insulating film of the wafer W. The results achieved in the individual implementation examples are presented in FIG. 3. FIG. 3(A) shows the state at the central area of the wafer W achieved in implementation example 2(a), FIG. 3(B) shows the state at the edge of the wafer W achieved in implementation example 2(a), FIG. 3(C) shows the state at the central area of the wafer W achieved in implementation example 2(b) and FIG. 3(D) shows the state at the edge of the wafer W achieved in implementation example 2(b).

As shown in FIG. 3, at the flow rate (a) $C_4F_8:N_2 = 12:200$, a high selection ratio and a good etching shape are achieved, whereas at the flow rate ratio (b) $C_4F_8:N_2 = 12:100$, the selection ratio is lower than that achieved at (a) and also an etching stop occurs.

Thus, among these implementation examples, the flow rate ratio (a) $C_4F_8:N_2 = 12:200$ achieves the most desirable results, and by comparing the results at (a) and (b), it can be judged that a higher selection and a good etching shape are achieved when the flow rate ratio is set essentially within a range of $10 \leq (N_2 \text{ flow rate} / C_4F_8 \text{ flow rate})$.

While the invention has been particularly shown and described with respect to preferred embodiments of the etching method according to the present invention by referring to the attached drawings, the present invention is not limited to these examples and it

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will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit, scope and teaching of the invention.

For instance, while an explanation is given above in reference to the embodiments and the implementation examples in which a processing gas achieved by mixing N_2 , C_4F_8 and Ar or a processing gas achieved by mixing N_2 , CF_4 and Ar is utilized, the present invention is not restricted by these particulars. For instance, the present invention may be implemented effectively even when Ar is not contained in the processing gas or when an inert gas other than Ar is added into the processing gas. In other words, the present invention may be adopted successfully as long as the processing gas contains at least N_2 and C_4F_8 or at least N_2 and CF_4 .

In addition, while an explanation is given above in reference to the embodiments and the implementation examples in which a parallel-plane type etching apparatus is employed, the present invention is not limited by these structural particulars. The present invention may be adopted in any of various types of plasma etching apparatuses including an etching apparatus in which a magnetic field is formed inside the processing chamber, an inductively coupled etching apparatus provided with an electrostatic shield and a microwave type etching apparatus.

Furthermore, while an explanation is given above in reference to the embodiments and the implementation examples in which contact holes are formed at the layer insulating film formed at the wafer, the present invention is not restricted by these particulars, and it may be adopted to implement any type of etching process on a layer insulating film formed at a workpiece.

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As explained above, according to the present invention, improvements in the selection ratio and the etching shape are achieved.

The entire disclosure of Japanese Patent Application No. 11-303422 filed on October 26, 1999 including specification, claims, drawings and summary is incorporated herein by reference in its entirety.

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What is claimed is;

1. An etching method for etching an etching target film formed on a substrate placed inside an airtight processing chamber by inducing a processing gas into said processing chamber, wherein;
said processing gas contains, at least, CF_4 and N_2 ; and
said etching target film is constituted of an upper organic film containing Si and a lower SiO_2 film.
2. An etching method according to claim 1, wherein;
said organic film containing Si is constituted of SiO_2 containing C and H.
3. An etching method according to claim 1, wherein;
the dielectric constant of said organic film containing Si is equal to or lower than 3.0.
4. An etching method according to claim 1, wherein;
said organic film containing Si is an organic polysiloxane film.
5. An etching method according to claim 1, wherein;
said processing gas further contains Ar.
6. An etching method according to claim 1, wherein;
the flow rate ratio of CF_4 and N_2 in said processing gas is essentially set within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$.
7. An etching method for etching an etching target film formed on a substrate placed inside an airtight processing chamber by inducing a processing gas into said processing chamber, wherein;
said processing gas contains, at least, C_2F_6 and N_2 ; and

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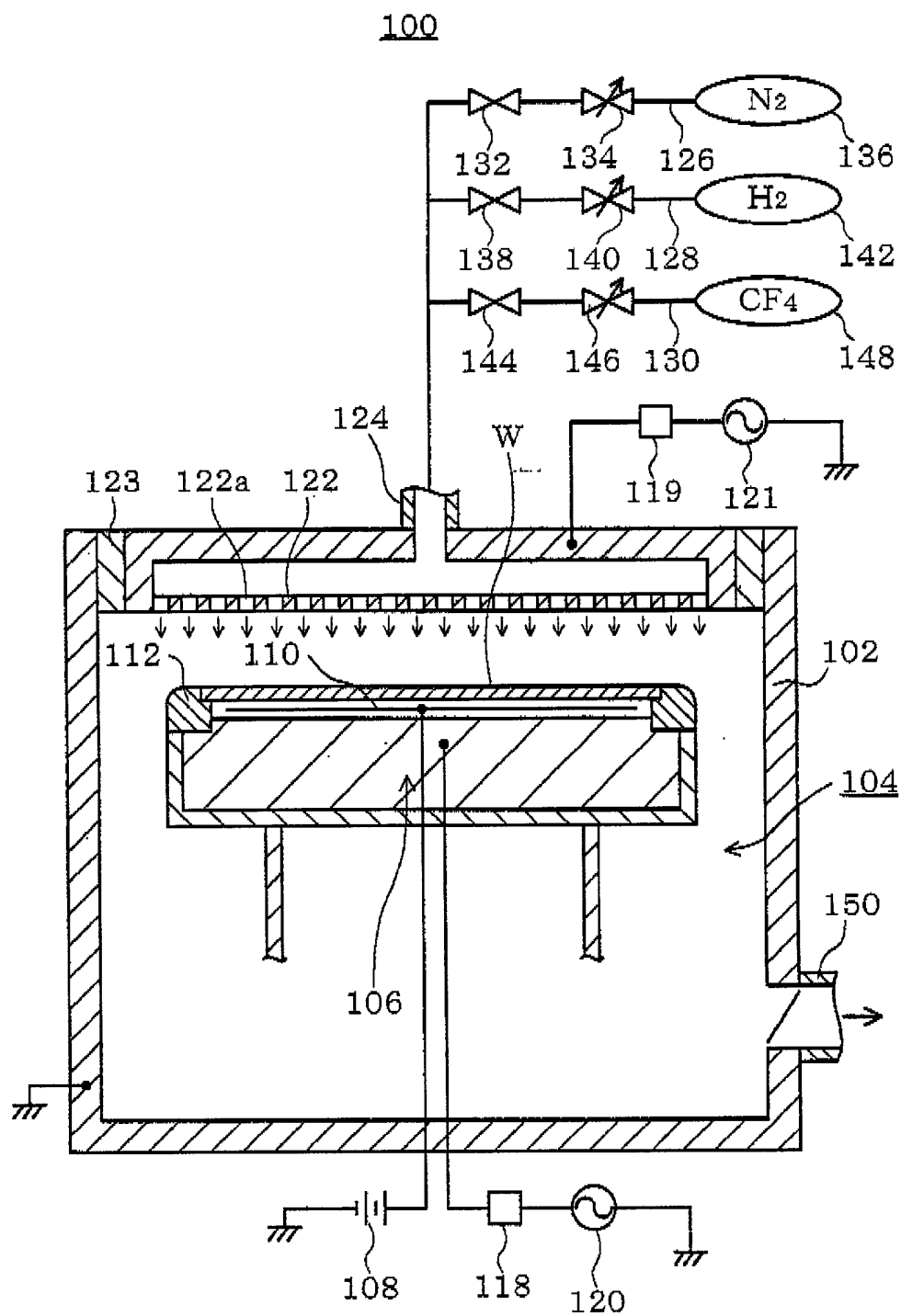
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Abstract of the Disclosure

In an etching method for etching an etching target film formed on a substrate placed inside an airtight processing chamber 104 by inducing a processing gas into the processing chamber 104, the processing gas contains CF_4 , N_2 and Ar and the etching target film is constituted of an upper organic polysiloxane film and a lower inorganic SiO_2 film. The flow rate ratio of CF_4 and N_2 in the processing gas is essentially set within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$. If $(\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate})$ is less than 1, an etching stop occurs and, as a result, deep etching is not achieved. If, on the other hand, $(\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate})$ is larger than 4, bowing tends to occur and, thus, a good etching shape is not achieved. Accordingly, the flow rate ratio of CF_4 and N_2 in the processing gas should be set essentially within a range of $1 \leq (\text{N}_2 \text{ flow rate} / \text{CF}_4 \text{ flow rate}) \leq 4$, to ensure that improvements in both the selection ratio and the etching shape are achieved.

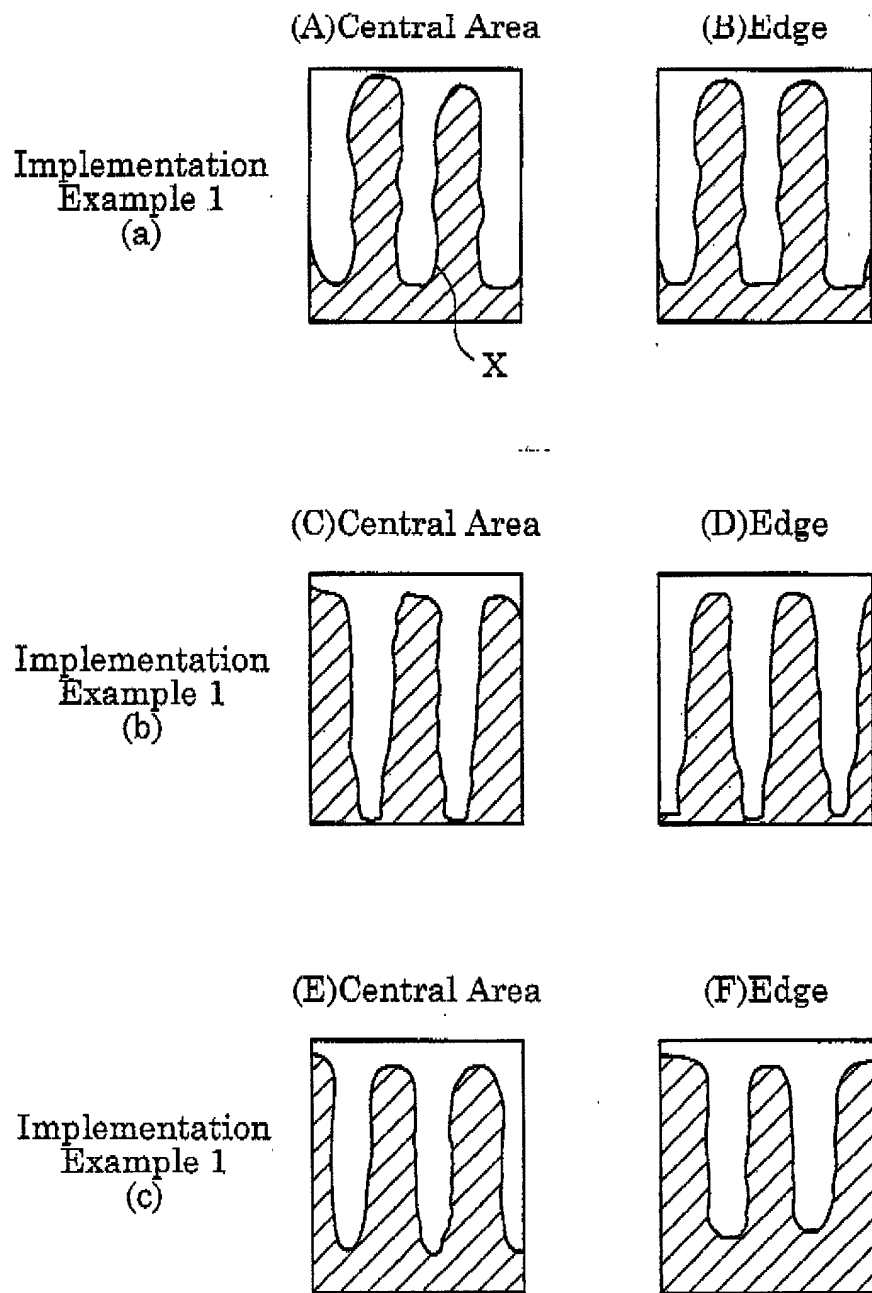
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FIG.1



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FIG.2

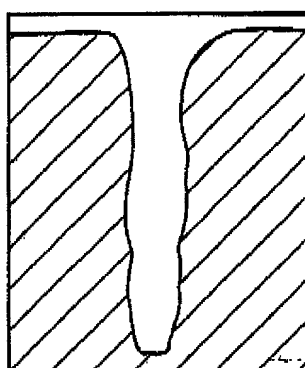


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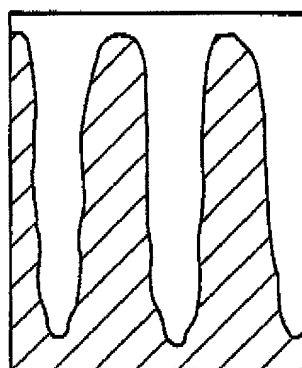
FIG.3

Implementation
Example 2
(a)

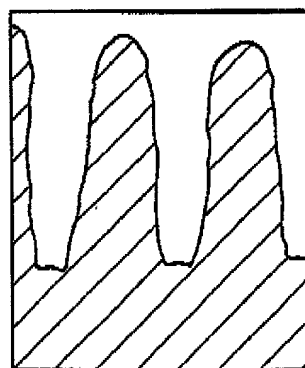
(A)Central Area



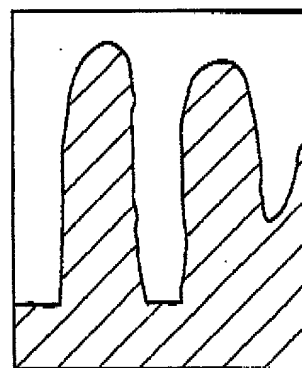
(B)Edge



(C)Central Area



(D)Edge



Implementation
Example 2
(b)

Attorney Docket No. _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: Etching Method

_____ the specification of which ☒ is attached and/or ☐ was filed on _____ as United States Application Serial No. _____ or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT International application(s) designating at least one country other than the United States, listed below and have also identified below, any foreign application(s) for patent or inventor's certificate, or any PCT International application(s) having a filing date before that of the application(s) of which priority is claimed:

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C.
Japan	JP11-303422	October 26, 1999	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Number	Date of Filing

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) or § 365(c) of any PCT International application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application(s) and the national or PCT International filing date of this application:

Application Number	Date of Filing	Status (Patented, Pending, Abandoned)

I hereby appoint the following attorney and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., Douglas B. Henderson, Reg. No. 20,291; Ford F. Farabow, Jr., Reg. No. 20,630; Arthur S. Garrett, Reg. No. 20,339; Donald R. Dunner, Reg. No. 19,073; Brian G. Brunsvold, Reg. No. 22,593; Tipton D. Jennings, IV, Reg. No. 20,645; Jerry D. Voight, Reg. No. 23,020; Laurence R. Heffter, Reg. No. 20,827; Kenneth E. Payne, Reg. No. 23,098; Herbert H. Mintz, Reg. No. 26,691; C. Larry O'Rourke, Reg. No. 26,014; Albert J. Santorelli, Reg. No. 22,610; Michael C. Elmer, Reg. No. 25,857; Richard H. Smith, Reg. No. 20,609; Stephen L. Peterson, Reg. No. 26,325; John M. Romary, Reg. No. 26,331; Bruce C. Zotter, Reg. No. 27,680; Dennis P. O'Reilly, Reg. No. 27,932; Allen M. Sokal, Reg. No. 26,695; Robert D. Bajefsky, Reg. No. 25,387; Richard L. Stroup, Reg. No. 28,478; David W. Hill, Reg. No. 28,220; Thomas L. Irving, Reg. No. 28,619; Charles E. Lipsey, Reg. No. 28,165; Thomas W. Winland, Reg. No. 27,605; Basil J. Lewis, Reg. No. 28,818; Martin I. Fuchs, Reg. No. 28,508; E. Robert Yoches, Reg. No. 30,120; Barry W. Graham, Reg. No. 29,924; Susan Haberman Griffen, Reg. No. 30,907; Richard B. Racine, Reg. No. 30,415; Thomas H. Jenkins, Reg. No. 30,857; Robert E. Converse, Jr., Reg. No. 27,432; Clair X. Mullen, Jr., Reg. No. 20,348; Christopher P. Foley, Reg. No. 31,354; John C. Paul, Reg. No. 30,413; Roger D. Taylor, Reg. No. 28,992; David M. Kelly, Reg. No. 30,953; Kenneth J. Meyers, Reg. No. 25,146; Carol P. Einaudi, Reg. No. 32,220; Walter Y. Boyd, Jr., Reg. No. 31,738; Steven M. Anzalone, Reg. No. 32,095; Jean B. Fordis, Reg. No. 32,984; Barbara C. McCurdy, Reg. No. 32,120; James K. Hammond, Reg. No. 31,964; Richard V. Burgullan, Reg. No. 31,744; J. Michael Jakes, Reg. No. 32,824; Thomas W. Banks, Reg. No. 32,719; Christopher P. Isaac, Reg. No. 32,616; Bryan C. Diner, Reg. No. 32,409; M. Paul Barker, Reg. No. 32,013; Andrew Chanho Sonu, Reg. No. 33,457; David S. Forman, Reg. No. 33,694; Vincent P. Kovalick, Reg. No. 32,867; James W. Edmondson, Reg. No. 33,871; Michael R. McGurk, Reg. No. 32,045; Joann M. Neth, Reg. No. 36,363; Garson S. Panitch, Reg. No. 33,751; Cheryl M. Taylor, Reg. No. 33,216; Charles E. Van Horn, Reg. No. 40,266; Linda A. Wadler, Reg. No. 33,218; Jeffrey A. Berkowitz, Reg. No. 36,743; Michael R. Kelly, Reg. No. 33,921; James B. Monroe, Reg. No. 33,971; Doris Johnson Hines, Reg. No. 34,629; Allen R. Jensen, Reg. No. 28,224; Lori Ann Johnson, Reg. No. 34,498; and David A. Manspelzer, Reg. No. 37,540 and _____. Please address all correspondence to FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P. 1300 I Street, N.W., Washington, D.C. 20005, Telephone No. (202) 408-4000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Attorney Docket No. _____

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Residence	Yamanashi, Japan			Citizenship	Japanese
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Full Name of Fourth Inventor	Inventor's Signature		Date		
Residence			Citizenship		
Post Office Address					
Full Name of Fifth Inventor	Inventor's Signature		Date		
Residence			Citizenship		
Post Office Address					
Full Name of Sixth Inventor	Inventor's Signature		Date		
Residence			Citizenship		
Post Office Address					
Full Name of Seventh Inventor	Inventor's Signature		Date		
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Residence			Citizenship		
Post Office Address					
Full Name of Ninth Inventor	Inventor's Signature		Date		
Residence			Citizenship		
Post Office Address					

Listing of Inventors Continued on Page 2 hereof. ☐ Yes ☐ No

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

January 2000